Fibocom
PERFECT WIRELESS EXPERIENCE

FG132-MiniPCIe Hardware Guide

V1.3

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Contact Information

Website: https://www.fibocom.com

Address: 10/F-14/F, Block A, Building 6, Shenzhen International Innovation Valley, Dashi First Road, Xili Community, Xili Subdistrict, Nanshan District, Shenzhen

Tel: 0755-26733555

Contents

Applicable Models

No.	Applicability Model	Description
1.	FG132-GL-00-MiniPCIe-00	5G Redcap, 4G/5G, 2Gb DDR2+2GB FLASH, Global band, Master set, Diversity, GNSS antenna, Standard
2.	FG132-CN-00-MiniPCIe-00	5G Redcap, 4G/5G, 2Gb DDR2+2GB FLASH, Domestic band, Master set, Diversity, GNSS antenna, Standard
3.	FG132-GL-00-MiniPCIe-10	5G Redcap, 4G/5G, 2Gb DDR2+2GB FLASH, Global band, Master set, Diversity, Active GNSS antenna, Standard

Change History

V1.3 (2024-11-25)	Updated power consumption data and added edrx power, size refresh
V1.2 (2024-07-23)	Updated power consumption data and added applicable models
V1.1 (2024-04-27)	Updated the RF indicator and added the GNSS indicator
V1.0 (2024-02-08)	Initial version

1 Foreword

1.1 Description

By reading this document, you can quickly understand the interface specifications, electrical characteristics, mechanical dimensions and other special requirements of the module. Combined with our user guide, customers can quickly design and debug the wireless part of the circuit.

1.2 Reference Standards

This product is designed with reference to the following standards:

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- 3GPP TS 36.521-1 V15.0.0：User Equipment （UE） conformance specification; Radio transmission and reception; Part 1：Conformance testing
- 3GPP TS 38.300 V15.5.0 ： 3rd Generation Partnership Project; Technical Specification Group Radio Access Network; NR; NR and NG-RAN Overall Description; Stage 2
- 3GPP TS 38.521-1 V15.2.0 ： User Equipment （UE） conformance specification; Radio transmission and reception; Part 1： Range 1 Standalone;
- 3GPP TS 38.521-3 V15.2.0：User Equipment （UE） conformance specification; Radio transmission and reception; Part 3：Range 1 and Range 2 Interworking operation with other radios;
- 3GPP TS 36.124V10.3.0：Electro Magnetic Compatibility（EMC）requirements for mobile terminals and ancillary equipment
- 3GPP TS 21.111 V10.0.0：USIM and IC card requirements
- 3GPP TS 51.011 V4.15.0：Specification of the Subscriber Identity Module -Mobile Equipment （SIM-ME） interface
- 3GPP TS 31.102 V10.11.0：Characteristics of the Universal Subscriber Identity Module （USIM） application
- 3GPP TS 31.11 V10.16.0：Universal Subscriber Identity Module（USIM）Application Toolkit（USAT）
- 3GPP TS 27.007 V10.0.8：AT command set for User Equipment（UE）
- 3GPPTS27.005 V10.0.1：Use of Data Terminal Equipment -Data Circuit terminating Equipment （DTE - DCE）interface for Short Message Service（SMS）and Cell Broadcast Service （CBS）
- Universal Serial Bus Specification 2.0

2 Product Overview

2.1 General Description

FG132 MiniPCIe series is a highly integrated 5G wireless communication module that uses a standard MiniPCIe interface and supports 5G NR/LTE network standards. The module can provide stable and high-speed data transmission service, which is suitable for most mobile operator networks in the world, and can be widely used in industrial gateways and IPC scenarios.

Table 1. Operating bands

Model	Antenna Quantity	Network standard	Band Configuration
FG132-GL-00	3	5G NR	SA: n1/2/3/5/7/8/12/13/14/18/20/25/26/28/30/38/40/41/48/66/70/71/77/78
		LTE	LTE: B1/2/3/4/5/7/8/12/13/14/17/18/19/20/25/26/28/30/34/38/39/40/41/42/43/48/66/71
		GNSS	GPS/GLONASS/BDS/Galileo/QZSS
FG132-CN-00	3	5G NR	SA: n1/3/5/8/28/40/41/78/79
		LTE	LTE: B1/3/5/8/34/38/39/40/41
		GNSS	GPS/GLONASS/BDS/Galileo/QZSS

2.2 Key Features

Table 2. Key features

Category	Function Description
Power supply	DC: 3.3V to 4.3V; typical value: 3.8V
Operating system of host computer	Linux / Android / Windows
Network protocol	IPv4/IPv6
SMS	Supported
Memory	2Gb DDR2 + 2Gb NAND Flash
Function interface	USIM x1, Supports 3V/1.8V cards and hot swap
	USB x1: USB2.0, used for AT command communication, data transmission, software debugging, and firmware upgrade
	PCM x1: Audio function for external Codec; Support 16-bit linear data

Category	Function Description	
	format; Support long frame synchronization and short frame synchronization; Support for master mode and slave mode *	
	Antenna x3: main set, diversity, and GNSS antennas	
LTE features	UL supports QPSK, 16QAM and 64QAM modulations DL supports QPSK, 16QAM, 64QAM and 256QAM modulations LTE: A maximum uplink rate of 75Mbps and a maximum downlink rate of 195Mbps	
5G NR features	UL supports QPSK, 16QAM, 64QAM, 256QAM and PI/2 BPSK modulations DL supports QPSK, 16QAM, 64QAM and 256QAM modulations A maximum uplink rate of 123 Mbps and a maximum downlink rate of 223 Mbps	
RF Power level	5G NR Band: Class 3 (23 dBm ±2 dB) LTE Band: Class 3 (23 dBm ±2 dB)	
	LTE HPUE Band	Class 2 (26 dBm ±2 dB)
		FG132-GL-00：B38/40/41/42/43
		FG132-CN-00：B38/41
5G SRS	Support 1T2R FG132-GL-00：n38/41/48/77/78 FG132-CN-00：n40/41/78/79	
GNSS features	Supports dual-band GNSS: L1/L5 Supports GPS, GLONASS, BDS, Galileo/ QZSS Supports Gen 9 v5.1 engine Protocol: NMEA 0183 Data update rate: 1 Hz by default	
Physical characteristics	Dimension: (50.8±0.15)mm×(29.85±0.15)mm×(3.4±0.3)mm Encapsulation: MINIPCIE Weight: about 10g	
Temperature characteristics	Operating temperature: –35°C~+75°C. The module can work normally and meet the requirements of 3GPP standard. Extended temperature: –40°C~+85°C. The module can work normally, and some performance indicators may exceed the requirements of 3GPP standard. Storage temperature: -45°C~+90°C, normal storage temperature range when the module is not powered on.	

Category	Function Description
Upgrade Software	By USB/FOTA
Environmental protection standard	RoHS, HF

2.3 Hardware Block Diagram

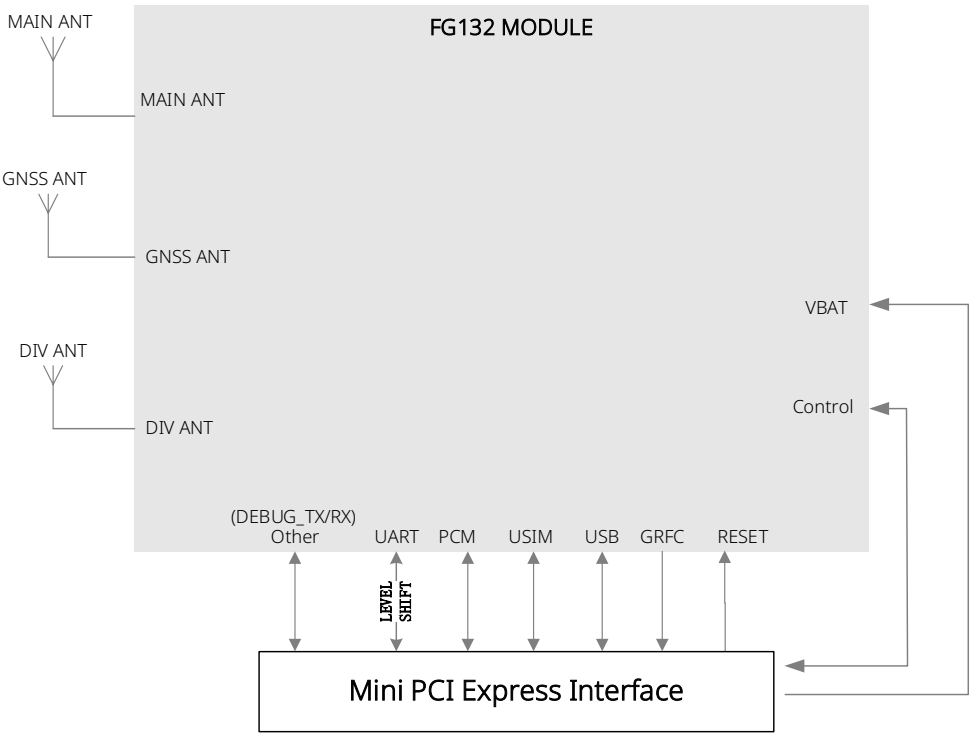


Figure 1. Hardware block diagram

The above figure is the hardware block diagram of the module, which mainly introduces the key components and functions of the baseband and radio frequency parts.

- MiniPCIe Interface
- FG132 Module
- MAIN ANT
- DIV ANT
- GNSS ANT

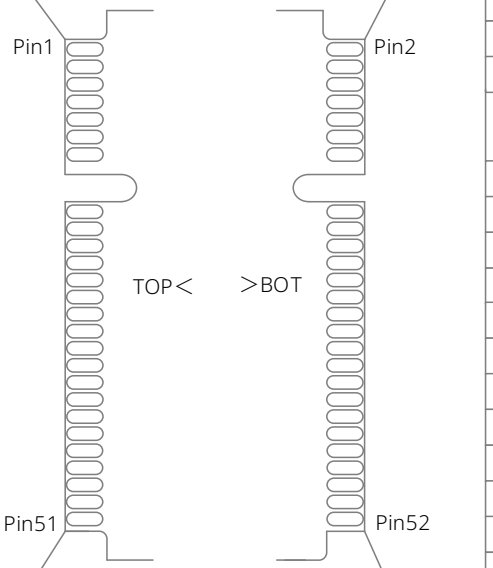
2.4 Description of Development kit

Fibocom configures a complete development kit for the module, which is convenient for users to quickly understand the performance of the module. For details about development board usage, see the *Fibocom_EVK-GT8230-NL_User Guide.*

3 Pin Definition

3.1 Pin Distribution

Pin Name	Pin Num
WAKE#	1
RESERVED	3
RESERVED	5
RESERVED	7
GND	9
UART_RX	11
UART_TX	13
GND	15
UART_RI	17
RESERVED	19
GND	21
UART_CTS	23
UART_RTS	25
GND	27
GND	29
UART_DTR	31
RESERVED	33
GND	35
GND	37
VCC_3V3	39
VCC_3V3	41
GND	43
PCM_CLK	45
PCM_DOUT	47
PCM_DIN	49
PCM_SYNC	51



Pin Num	Pin Name
2	VCC_3V3
4	GND
6	NC
8	USIM_VDD
10	USIM_DATA
12	USIM_CLK
14	USIM_RST
16	NC
18	GND
20	W_DISABLE#
22	PERST#
24	NC
26	GND
28	NC
30	I2C_SCL
32	I2C_SDA
34	GND
36	USB_DM
38	USB_DP
40	GND
42	LED_WWAN#
44	USIM_PRESENCE
46	RESERVED
48	NC
50	GND
52	VCC_3V3

Figure 2. Pin distribution

3.2 Pin Description

Table 3. I/O type parameter definition

Type	Description	Type	Description
PI	Power input	AIO	Analog input and output
PO	Power output	OD	Open drain
DI	Digital input	PU	High level by pulling up
DO	Digital output	PD	Low level by pulling down
DIO	Digital input and output	T	Tristate, namely, high resistance, determined by

			the peripheral circuit
AI	Analog input	G	Ground
AO	Analog output	OC	Open collector

Table 4. Pin description

Pin No.	Pin Name	I/O	Reset Value1	DC Characteristics	Pin Description
1	WAKE#	- -	- -	3.3V	Hardware output wake up by default, 1, 17 pin choose one to use. Reserved input wake-up module.
2	VCC_3V3	PI	- -	3.3V to 4.3V	Module power supply
3	RESERVED	DI	PD	1.8V	The serial port of 5G/LTE and WLAN is reserved for receiving
4	GND	G	- -	- -	GND
5	RESERVED	DO	PD	1.8V	The 5G/LTE and WLAN serial ports are reserved for sending
6	NC	- -	- -	- -	- -
7	RESERVED	DI	PD	1.8V	Reserve AP_READY
8	USIM_VDD	PO	- -	1.8V/3V	(U)SIM power supply, the module automatically recognizes 1.8V or 3.0V SIM cards
9	GND	G	- -	- -	GND
10	USIM_DATA	DIO	Unstable	1.8V/3V	(U) The SIM data signal cable is pulled up internally
11	UART_RX	DI	PD	3.3V	Master serial reception
12	USIM_CLK	DO	Unstable	1.8V/3V	(U)SIM clock signal cable
13	UART_TX	DO	PD	3.3V	Master serial transmission
14	USIM_RST	DO	Unstable	1.8V/3V	(U) Signal cable for SIM reset
15	GND	G	- -	- -	GND
16	NC	- -	- -	- -	- -
17	UART_RI	DO	PD	3.3V	Ringing prompt
18	GND	G	- -	- -	GND
19	RESERVED	- -	- -	- -	Reserve
20	W_DISABLE#	DI	PD	3.3V	Module flight mode control, default pull-up, low level can

Pin No.	Pin Name	I/O	Reset Value1	DC Characteristics	Pin Description
					make the module into flight mode
21	GND	G	- -	- -	GND
22	PERST#	DI	- -	3.3V	Module reset signal, low level effective, no external pull-up required
23	UART_CTS	DI	PD	3.3V	The main serial port is cleared and sent
24	NC	- -	- -	- -	- -
25	UART_RTS	DO	PD	3.3V	Master serial port request sent
26	GND	G	- -	- -	GND
27	GND	G	- -	- -	GND
28	NC	- -	- -	- -	- -
29	GND	G	- -	- -	GND
30	I2C_SCL	OD	Unstable	1.8V	I2C clock signal
31	UART_DTR	DO	PD	3.3V	The host wakes up module
32	I2C_SDA	OD	PU	1.8V	I2C data signal
33	RESERVED	- -	- -	- -	The DBG_RXD serial port is reserved
34	GND	G	- -	- -	GND
35	GND	G	- -	- -	GND
36	USB_DM	AIO	- -	- -	USB differential data signal -
37	GND	G	- -	- -	GND
38	USB_DP	AIO	- -	- -	USB differential data signal +
39	VCC_3V3	PI	- -	3.3V to 4.3V	Module power supply
40	GND	G	- -	- -	GND
41	VCC_3V3	PI	- -	3.3V to 4.3V	Module power supply
42	LED_WWAN#	OC	PD	VBAT	Pilot signal
43	GND	G	- -	- -	GND
44	USIM_PRESENCE	DI	PD	1.8V	(U)SIM hot swap detection. The default high level is valid
45	PCM_CLK	DIO	PD	1.8V	PCM clock signal
46	RESERVED	- -	- -	- -	The DBG_TXD serial port is

Pin No.	Pin Name	I/O	Reset Value1	DC Characteristics	Pin Description
					reserved
47	PCM_DOUT	DO	PD	1.8V	PCM data output
48	NC	- -	- -	- -	- -
49	PCM_DIN	DI	PD	1.8V	PCM data entry
50	GND	G	- -	- -	GND
51	PCM_SYNC	DIO	PD	1.8V	PCM synchronization signal
52	VCC_3V3	PI	- -	3.3V to 4.3V	Module power supply

- Reset Value: Status of the pin during initialization.
- "*" indicates a reserved function, which has not been developed. If you need to use such a function, consult and communicate with Fibocom FAE.
- Unstable: Software is unstable for a period of time after the system starts. It is not recommended to connect a level-sensitive device.
- Pin 1 WAKE#, the hardware reserves output and input two modes, need to choose one to use, the priority to meet the output wake up. 1, 17 pin choose one to use.
- The output voltage domain is 1.8V and the input voltage domain is 3.3V.

4 Application Interfaces

4.1 Power Interface

4.1.1 Power pin Definition

Table 5. VBAT parameter

Pin Number	Pin Name	Min	Typical	Max	Unit
2,39,41,52	VBAT	3.3	3.8	4.3	V

4.1.2 Power Supply circuit

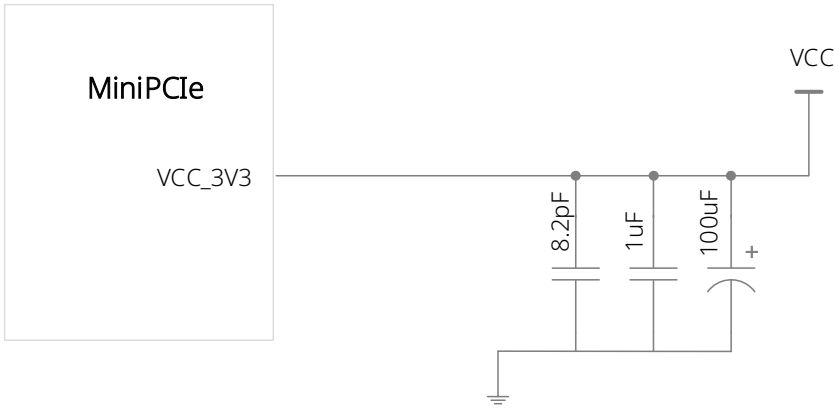


Figure 3. Reference circuit of power supply

The filter capacitor must be placed close to the power supply pin. The smaller the capacity, the closer it is to the corresponding power supply pin. The filter capacitor and the module are placed on the same side, do not cross the layer, otherwise there will be TIS interference risk, and the line is as short and wide as possible.

Table 6. Filter capacitance introduction

Design consideration	Way	Recommended parameter
Reduce power supply fluctuations during module operation	Voltage regulating capacitance	100uF(with low ESR capacitance)
Filter out interference from clock and digital signals	Filter capacitance	1uF
Eliminate high-low if RF interference	Decoupling capacitance	8.2pF

The recommended filter capacitor can be adjusted according to the actual situation, and the value is not fixed.

4.1.3 Voltage drop

The customer should choose a DC chip with a continuous output capability of greater than 2.6 A. The recommended input voltage of the module is 3.8 V, and the ripple should be less than 150 mV. Add a voltage stabilizing capacitor to ensure that the VBAT voltage will not continue to be lower than 3.3 V for more than 2ms during the operating of the module. Otherwise, the module will trigger the shutdown mechanism. The following figure shows the power supply requirements.

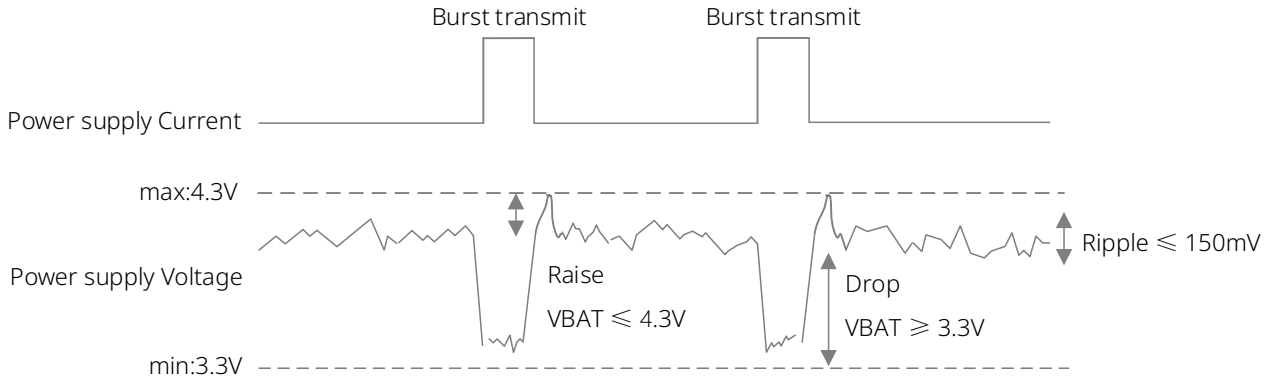


Figure 4. Power supply requirements

Due to the large peak current (about 2.6A) when the 5G module is operating, the VBAT voltage fluctuation will gradually decrease with the increase of the voltage stabilizing capacitor. However, it is impossible to eliminate the VBAT voltage fluctuation. Therefore, the power system of the module must be separated from the power supply of other main control chips to avoid voltage fluctuations affecting the power stability of the main control chip and causing the system to shut down.

4.2 Reset Interface

MINIPCIE defines two reset modes: hardware reset and software reset, which users can flexibly choose according to their own needs.

Table 7. Reset mode

Reset mode	Reset method
Hardware reset	Lower the RESET pin for 700ms to 1s. After the pin is released, the module starts the reset process
Software reset	Send the AT command AT+CFUN=15 to reset the module

The following focuses on the hardware reset circuit design and reset timing.

4.2.1 Reset Pin Definition

Table 8. Reset methods

Pin number	Pin name	I/O	Reset Value	Feature	DC Level
22	RESET_N	DI	PU	Module reset signal	1.8V

4.2.2 Resetting the circuit

The RESET_N pin is usually used to connect to the GPIO control pin on the AP side of the customer. The 1.8V pull-up module comes with itself, and no external pull-up is required. RESET_N is a sensitive signal. If it is not used, leave it blank. It is recommended to add a filter capacitor near the module to prevent jitter, keep away from interference when the PCB is running, and use GND protection. Keep the RESET_N signal cable away from the edge of the PCB and away from the surface to prevent abnormal module reset caused by ESD. The reset circuit is as follows:

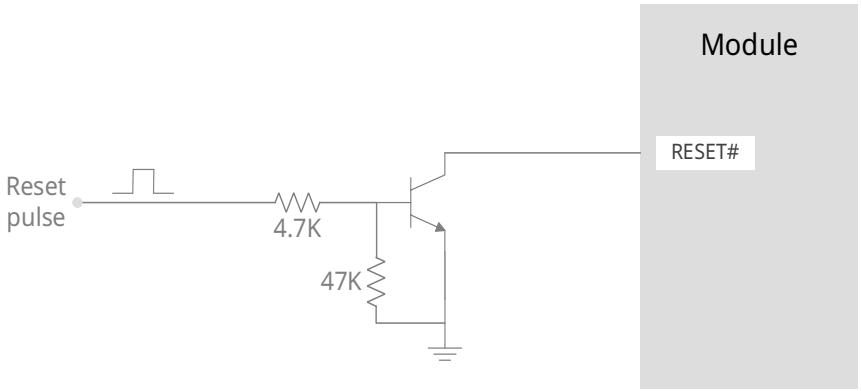


Figure 5. OC drive Reset circuit

- It is recommended to execute AT command to restart or shutdown first, and use RESET# only after a failed restart or shutdown.
- Ensure that RESET# do not have large load capacitance.

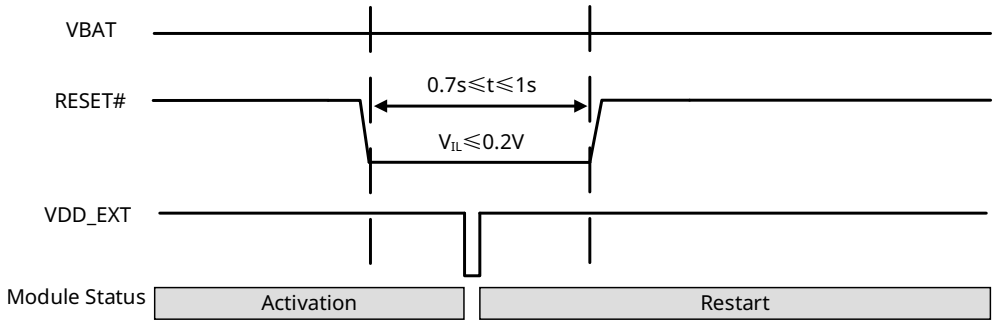


Figure 6. Reset timing sequence

4.3 USB Interface

The module provides a USB interface that conforms to the USB2.0 specification, supports high-speed mode, up to 480Mbps, and is backward compatible with 12Mbps full speed mode. The USB interface supports only slave mode and can be used for AT command communication, data transmission, software debugging, and firmware upgrade.

4.3.1 USB Pin Definition

Table 9. USB pin definition

Pin number	Pin name	I/O	Reset Value	Pin description
36	USB_DM	AIO	- -	USB 2.0 Differential data signal（-）
38	USB_DP	AIO	- -	USB 2.0 Differential data signal（+）

4.3.2 USB2.0 application circuit

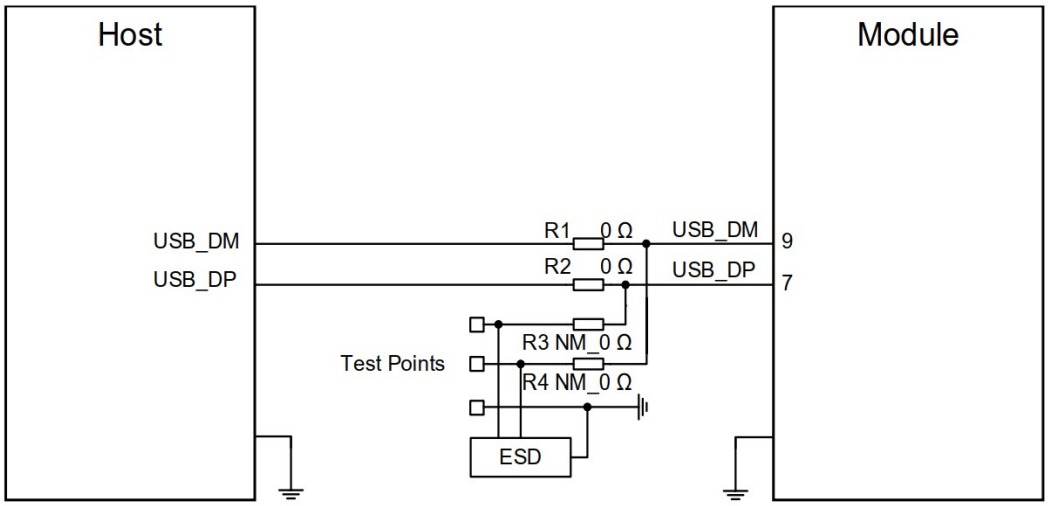


Figure 7. USB 2.0 reference design

It is recommended to series 0R resistor (co-pad with common-mode inductor) between host and module. In order to meet the signal integrity requirements of USB data lines, the common mode inductor should be placed close to the module, traces connecting test points should be kept as short as possible.

The USB 2.0 of the module includes both USB High-Speed (480Mbps) and USB Full-Speed (12Mbps) modes. The equivalent capacitance of the TVS diode on the differential signal lines should be less than 2pF. If there is no ESD risk for the USB interface, the TVS diode can be omitted.

Here are the layout design rules for USB 2.0:

- The differential impedance of USB_D- and USB_D+ signal lines should be controlled within 90Ω±10Ω.
- The length difference between the USB_D- and USB_D+ signal lines should be less than 2 mm, and they should be run in parallel. Avoid routing at right angles.
- It is recommended to route the USB_D- and USB_D+ signal lines on inner layers, with ground planes surrounding on the top, bottom, left and right sides of them for protection.

When not using the USB interface, it is recommended to use the USB 2.0 interface for firmware upgrades and reserve test points for debugging.

4.4 USIM Interface

One SIM card is built into the module

4.4.1 USIM Pin Definition

Table 10. USIM pin definition

Pin Number	Pin Name	I/O	Reset Value	Pin Description	DC Level
8	UIM1_VDD	PO	-	Power source	1.8V/3.0V
14	UIM1_RESET	DO	Unstable	Resetting	1.8V/3.0V
12	UIM1_CLK	DO	Unstable	Clock	1.8V/3.0V
10	UIM1_DATA	DIO	Unstable	Data	1.8V/3.0V
44	SIM1_DET	DI	PD	Detection	1.8V

4.4.2 USIM Interface circuit

The following is the reference design of the two SIM cards, among which the TVS tube is recommended to use ESDBL5V0A1 model, the circuit diagram is as follows:

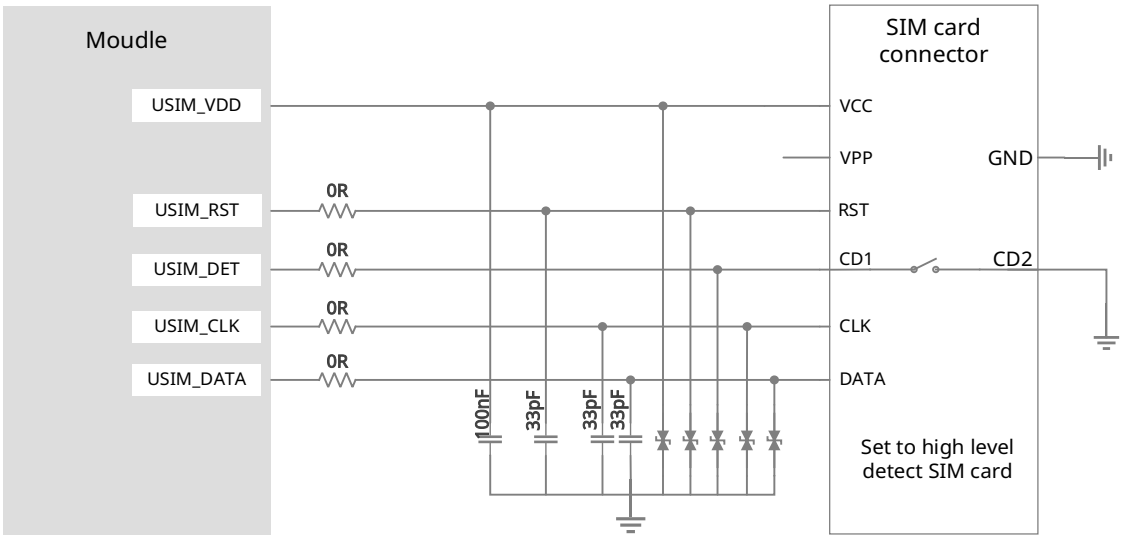


Figure 8. 8 pin SIM card reference circuit

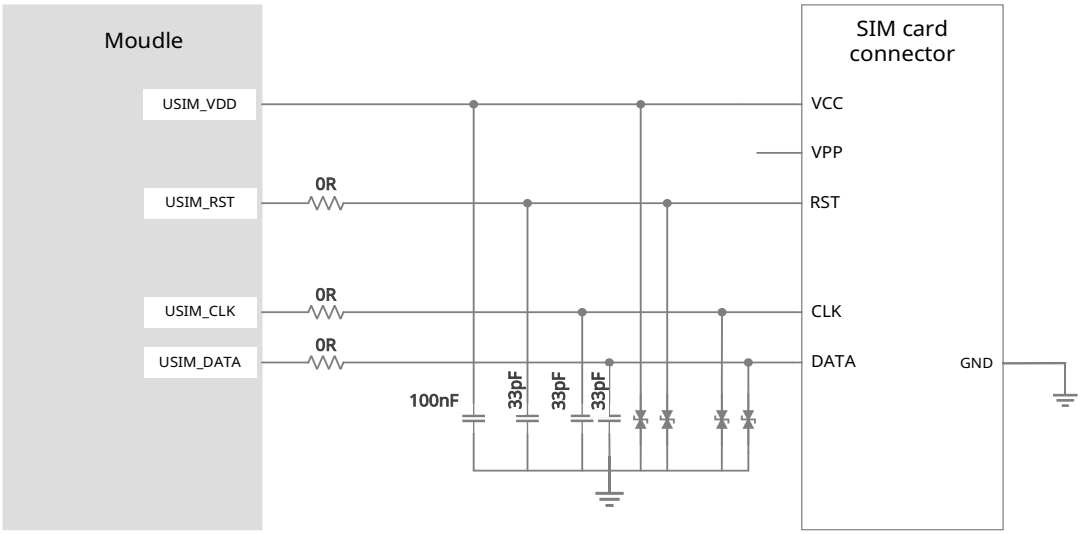


Figure 9. 6 pin SIM card reference circuit

The ESDBL5V0A1 model is recommended for TVS tubes in the above two SIM card reference designs. To ensure the stable operation of USIM cards, the following rules should be strictly followed in the design:

- Place the (U)SIM card slot close to the module and try to ensure that the length of the (U)SIM card signal trace does not exceed 200 mm.
- It is recommended to route (U)SIM card signal lines in the inner layer with a three-dimensional ground wrapped. It need to be kept away from power lines, crystals, magnetic devices, sensitive signals such as RF signals, analog signals, and noise signals generated by clocks and DC-DCs.
- To prevent crosstalk between the USIM_CLK signal and the USIM_DATA signal, the two traces should not be too close to each other, and a ground shield should be added between the two traces.
- (U)SIM card peripherals is placed as close as possible to the (U)SIM card slot. Add ESD protection devices near the card slot, and the parasitic capacitance of the selected TVS tube is not greater than 15pF. At the same time, a 0Ω resistor is connected in series between the module and the (U)SIM card slot for debugging. A 33pF capacitor is connected in parallel to the USIM_DATA, USIM_CLK, and USIM_RST signal lines to filter out RF interference.

4.4.3 USIM Hot Swap

The module implements hot plug function for the USIM card through the USIM_DET pin. A default high level represents that the SIM card is inserted, while a low level represents that the SIM card is removed. If the user does not need the hot plug function, float USIM_DET. In addition, the hot plug function of USIM card can be enabled and disabled by AT command.

Table 11. Hot plug function of USIM card

AT Command	Function Description	Note
AT+MSMPD=1	Enable the hot plug function detection of USIM card.	- -

AT+MSMPD=0	Disable the USIM card hot plug detection function.	- -

By default, the SIM hot swap function is enabled

4.5 PCM Interface

The module provides a set of PCM interfaces that support the following two modes:

- Short Frame Mode: The module can be slave* or master device.
- Long frame mode: The module can only be a master device.

The module supports 16-bit linear encoding formats. The following timing diagrams are for short frame mode (PCM_SYNC=8kHz, PCM_CLK=2048kHz) and long frame mode (PCM_SYNC=8kHz, PCM_CLK=256kHz).

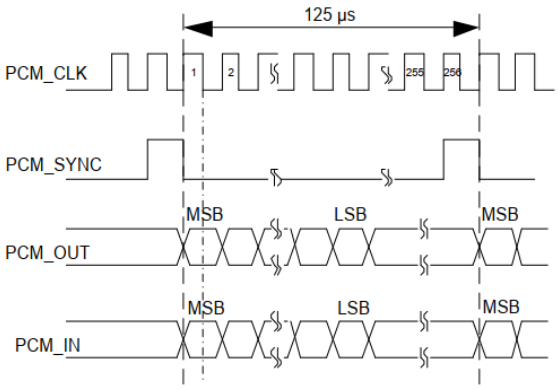


Figure 10. Timing diagram for short frame mode

In short frame mode, data is sampled on the falling edge of PCM_CLK and sent on the rising edge. The falling edge of PCM_SYNC represents a high valid bit. When PCM_SYNC reaches 8kHz, PCM_CLK supports 256kHz, 512kHz, 1024kHz and 2048kHz; when PCM_SYNC reaches 16kHz, PCM_CLK supports 4096kHz.

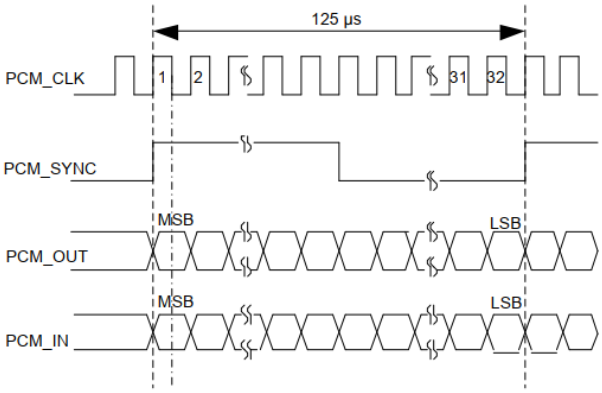


Figure 11. Timing diagram for short frame mode

In long frame mode, data is also sampled on the falling edge of PCM_CLK and sent on the rising edge. The rising edge of PCM_SYNC represents the high valid bit. When PCM_SYNC reaches 8kHz and the duty cycle is 50%, PCM_CLK supports 256kHz, 512kHz, 1024kHz, and 2048kHz.

- It is recommended that RC (R=22Ω, C=22pF) circuits be reserved on the signal lines of the PCM (especially PCM_CLK).
- The module can only be used as a master device in both PCM interface applications and I2C interface applications.

4.6 UART Interface

The module supports two UART interfaces, namely UART1 data transmission interface and DEG debugging interface. The interface functions are described as follows:

- UART1 Data transmission interface supports baud rates of 300bps,600bps,1200bps,2400bps, 4800bps, 9600bps, 19200bps, 38400bps, 57600bps, 115200bps (default), 230400bps, 460800bps, 921600bps. It is used to transmit data and send AT commands.
- DEG debugging interface supports a baud rate of 115200bps and is used to transmit logs.

4.6.1 UART Pin Definition

Table 12. UART pin definition

Pin Number	Pin Name	I/O	Reset Value	Pin Description	DC Level
11	UART1_RX	DI	PD	The main serial port receives data	3.3V
13	UART1_TX	DO	PD	The main serial port sends data	3.3V
17	UART1_RI	DO	PD	The module wakes up the host signal	3.3V
23	UART1_CTS	DI	PD	The main serial port is cleared and sent	3.3V
25	UART1_RTS	DO	PD	Master serial port sends request	3.3V

Pin Number	Pin Name	I/O	Reset Value	Pin Description	DC Level
31	UART1_DTR	DI	PD	The host wakes up module	3.3V
33	DBG_RXD*	DI	PD	DEBUG serial port reception	1.8V
46	DBG_TXD*	DO	Unstable	DEBUG serial port sending	1.8V

Pins marked with * are reserved.

4.7 Network State Indicator Interface

4.7.1 Definition of indicator lamp pin

Table 13. Network status indicator pin definition

Pin Number	Pin Name	I/O	Reset Value	Pin Description
42	LED_WWAN#	OC	PD	System status LED

4.7.2 Network status indicator circuit

The following figure shows the LED driver circuit.

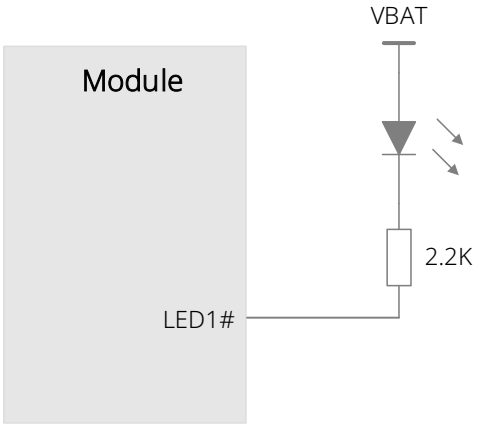


Figure 12. Reference circuit for the network status indicator

The following table describes the working status of the LED_WWAN# signal.

Table 14. Working status of the LED signal

Pin Name	Module Operating Mode	LED1# Signal

LED_WWAN#	RF function ON	Low level (LED On)
	RF function OFF	High level (LED Off)

4.8 Flight Mode Control Interface

Table 15. Flight mode control pin definition

Pin Number	Pin Name	I/O	Reset Value	Pin Description
20	W_DISABLE#	I	PD	Module flight mode control pin

The module supports two flight mode control methods:

- AT command control method:

  The software defaults to this control method. When the AT+CFUN=0 command is sent, the module enters the flight mode. When the AT+CFUN=1 command is sent, the module enters the operating mode.

- Hardware control method:

  This function is disabled by default. It can be enabled by sending the AT+GTFMODE=1 command through USB. There is a pull-up resistor inside the W_DISABLE1# module by default. When the pin of W_DISABLE1# is pulled up, the module enters the operating mode. When the pin of W_DISABLE1# is pulled down, the module enters the flight mode. This function can be disabled by using the AT+GTFMODE=0 command.

5 Antenna Interface

5.1 Antenna Interface Definition

The following table contains all the frequency bands of the series. Please read the definition of the antenna interface carefully and choose the correct antenna interface to connect. If you need other help, contact the Fibocom FAE.

Table 16. Definition of antenna interfaces

Connector	Function Description	TX	RX	Frequency Range
MAIN ANT	TRX	LTE: B1/2/3/4/5/7/8/12/13/14/17/18/19/20/25/26/28/30/B34/38/39/40/41/42/43/48/66/71 NR: n1/2/3/5/7/8/12/13/14/18/20/25/26/28/30/38/40/41/48/66/70/71/77/78/79	LTE: B1/2/3/4/5/7/8/12/13/14/17/18/19/20/25/26/28/30/B34/38/39/40/41/42/43/48/66/71 NR: n1/2/3/5/7/8/12/13/14/18/20/25/26/28/30/38/40/41/48/66/70/71/77/78/79	617MHz~5GHz
DIV ANT	DRX	- -	LTE: B1/2/3/4/5/7/8/12/13/14/17/18/19/20/25/26/28/30/B34/38/39/40/41/42/43/48/66/71 NR: n1/2/3/5/7/8/12/13/14/18/20/25/26/28/30/38/40/41/48/66/70/71/77/78/79	617MHz~5GHz
GNSS ANT	GNSS	- -	GPS/GLONASS/BDS/Galileo/QZSS	1166MHz~1606MHz

5.2 Operating Bands

Table 17. Cellular frequency reference table

Mode	Band	TX (MHz)	RX (MHz)
NR FDD	n1	1920~1980	2110~2170
	n2	1850~1910	1930~1990
	n3	1710~1785	1805~1880
	n5	824~849	869~894

Mode	Band	TX (MHz)	RX (MHz)
	n7	2500~2570	2620~2690
	n8	880~915	925~960
	n12	699~716	729~746
	n13	777~787	746~756
	n14	788~798	758~768
	n18	815~830	860~875
	n20	832~862	791~821
	n25	1850~1915	1930~1995
	n26	814~849	859~894
	n28	703~748	758~803
	n30	2305~2315	2350~2360
	n66	1710~1780	2110~2180
	n70	1695~1710	1995~2010
	n71	663~698	617~652
NR TDD	n38	2570~2620	2570~2620
	n40	2300~2400	2300~2400
	n41	2496~2690	2496~2690
	n48	3550~3700	3550~3700
	n77	3300~4200	3300~4200
	n78	3300~3800	3300~3800
	n79	4400~5000	4400~5000
LTE FDD	Band 1	1920~1980	2110~2170
	Band 2	1850~1910	1930~1990
	Band 3	1710~1785	1805~1880
	Band 4	1710~1755	2110~2155
	Band 5	824~849	869~894
	Band 7	2500~2570	2620~2690
	Band 8	880~915	925~960
	Band 12	699~716	729~746
	Band 13	777~787	746~756
	Band 14	788~798	758~768

Mode	Band	TX (MHz)	RX (MHz)
	Band 17	704~716	734~746
	Band 18	815~830	860~875
	Band 19	830~845	875~890
	Band 20	832~862	791~821
	Band 25	1850~1915	1930~1995
	Band 26	814~849	859~894
	Band 28	703~748	758~803
	Band 30	2305~2315	2350~2360
	Band 66	1710~1780	2110~2180
	Band 71	663~698	617~652
LTE TDD	Band 34	2010~2025	2010~2025
	Band 38	2570~2620	2570~2620
	Band 39	1880~1920	1880~1920
	Band 40	2300~2400	2300~2400
	Band 41	2496~2690	2496~2690
	Band 42	3400~3600	3400~3600
	Band 43	3600~3800	3600~3800
	Band 48	3550~3700	3550~3700

5.3 Antenna Performance Requirements

Input impedance: 50 Ω

Input power: > 28 dBm

VSWR: < 2:1

Antenna gain: < 3.6 dBi

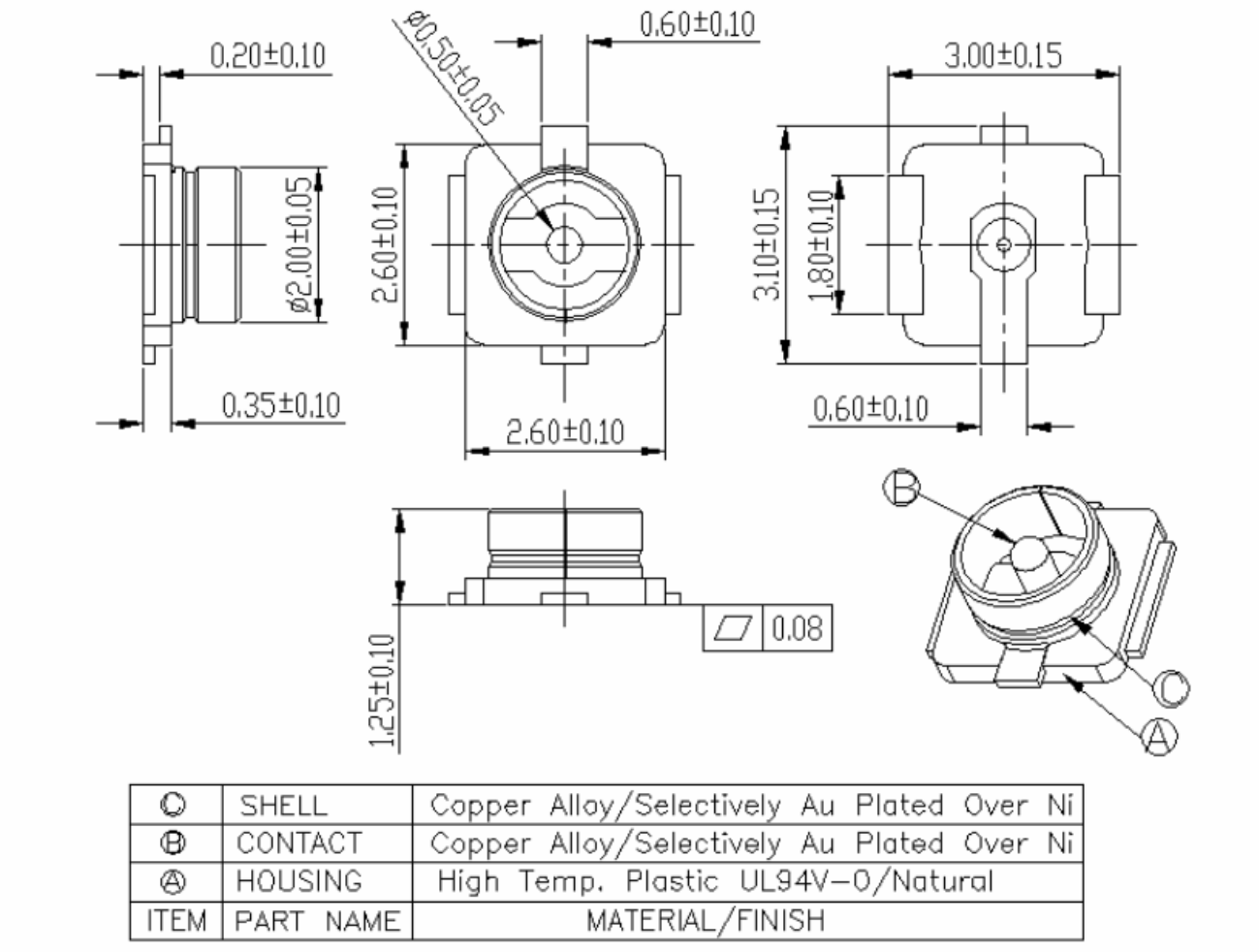
Antenna Isolation: > 25 dB

Antenna cable insertion loss: LB (< 1 GHz) < 0.3 dB, MB (1–2.7 GHz) < 0.8 dB, HB (> 2.7 GHz) < 1.2 dB

Minipci-00 GNSS supports only passive antennas; Minipci-10 GNSS supports only active antennas, and the operating voltage of active antennas should be within 3.4V-4.3V.

5.4 RF Connector

The frequency range of RF connectors is DC to 6GHz, the characteristic impedance is 50Ω, and the operating temperature range is -40 °C to +85°C. In order to facilitate the user to connect the antenna, the module comes with RF connector. The model is ECT 818000368, the size is 3.0X3.1X1.25mm, and the connector size is shown in the following figure:



ITEM	PART NAME	MATERIAL/FINISH
Ⓒ	SHELL	Copper Alloy/Selectively Au Plated Over Ni
Ⓑ	CONTACT	Copper Alloy/Selectively Au Plated Over Ni
Ⓐ	HOUSING	High Temp. Plastic UL94V-0/Natural

Figure 13. RF connector dimensions

6 Electrical Characteristics

6.1 Logic Level

Table 18. Logic level

Description	Level	Min.	Typical	Max.	Unit
1.8 V logic Level	Digital High level input	1.26	1.8	2.1	V
	Digital Low level input	-0.3	0	0.54	V
	Digital High level output	1.35	1.8	1.8	V
	Digital Low level output	0	0	0.45	V

6.2 Power Consumption

The power consumption measurement is closely related to the operating status of the module. The test conditions are as follows:

The ambient temperature is 25℃, and the power supply voltage is 3.8 V. The USB interface of the module defaults to the Device mode.

Table 19. Power consumption

Parameter	Mode	Condition	Current (mA)
I_{sleep}	Radio off	AT+CFUN=0 AT+SLPMODE=1	3.6
	NR FDD	Paging cycle #64 frames (USB Disconnect)	4.5
		Paging cycle #64 frames (USB Suspend)	5.3
		Paging cycle #128 frames (USB Disconnect)	4.2
		Paging cycle #128 frames (USB Suspend)	5.0
		Paging cycle #256 frames (USB Disconnect)	4.0
		Paging cycle #256 frames (USB Suspend)	4.8
		EDRX=20.48s, PTW=1.28s, DRX=1.28s (USB Disconnect)	3.8
		EDRX=20.48s, PTW=1.28s, DRX=1.28s (USB Suspend)	4.6
		EDRX=40.96s, PTW=1.28s, DRX=1.28s (USB Disconnect)	3.7
		EDRX=40.96s, PTW=1.28s, DRX=1.28s (USB Suspend)	4.5
		EDRX=81.92s, PTW=1.28s, DRX=1.28s (USB Disconnect)	3.6
		EDRX=81.92s, PTW=1.28s, DRX=1.28s (USB Suspend)	4.4

		EDRX=81.92s, PTW=2.56s, DRX=1.28s (USB Disconnect)	3.6
		EDRX=81.92s, PTW=2.56s, DRX=1.28s (USB Suspend)	4.4
	NR TDD	Paging cycle #64 frames (USB Disconnect)	4.5
		Paging cycle #64 frames (USB Suspend)	5.3
		Paging cycle #128 frames (USB Disconnect)	4.2
		Paging cycle #128 frames (USB Suspend)	4.9
		Paging cycle #256 frames (USB Disconnect)	4
		Paging cycle #256 frames (USB Suspend)	4.7
		EDRX=20.48s, PTW=1.28s, DRX=1.28s (USB Disconnect)	3.8
		EDRX=20.48s, PTW=1.28s, DRX=1.28s (USB Suspend)	4.6
		EDRX=40.96s, PTW=1.28s, DRX=1.28s (USB Disconnect)	3.7
		EDRX=40.96s, PTW=1.28s, DRX=1.28s (USB Suspend)	4.5
		EDRX=81.92s, PTW=1.28s, DRX=1.28s (USB Disconnect)	3.6
		EDRX=81.92s, PTW=1.28s, DRX=1.28s (USB Suspend)	4.4
		EDRX=81.92s, PTW=2.56s, DRX=1.28s (USB Disconnect)	3.6
		EDRX=81.92s, PTW=2.56s, DRX=1.28s (USB Suspend)	4.4
	LTE FDD	Paging cycle #64 frames (USB Disconnect)	4.3
		Paging cycle #64 frames (USB Suspend)	5.1
		Paging cycle #128 frames (USB Disconnect)	4.1
		Paging cycle #128 frames (USB Suspend)	4.9
		Paging cycle #256 frames (USB Disconnect)	4
		Paging cycle #256 frames (USB Suspend)	4.9
		EDRX=20.48s, PTW=1.28s, DRX=1.28s (USB Disconnect)	4
		EDRX=20.48s, PTW=1.28s, DRX=1.28s (USB Suspend)	4.8
		EDRX=40.96s, PTW=1.28s, DRX=1.28s (USB Disconnect)	3.9
		EDRX=40.96s, PTW=1.28s, DRX=1.28s (USB Suspend)	4.7
		EDRX=81.92s, PTW=1.28s, DRX=1.28s (USB Disconnect)	3.9
		EDRX=81.92s, PTW=1.28s, DRX=1.28s (USB Suspend)	4.7
		EDRX=81.92s, PTW=2.56s, DRX=1.28s (USB Disconnect)	3.9
		EDRX=81.92s, PTW=2.56s, DRX=1.28s (USB Suspend)	4.7
	LTE TDD	Paging cycle #64 frames (USB Disconnect)	4.3
		Paging cycle #64 frames (USB Suspend)	5.1

		Paging cycle #128 frames (USB Disconnect)	4.1
		Paging cycle #128 frames (USB Suspend)	4.9
		Paging cycle #256 frames (USB Disconnect)	4
		Paging cycle #256 frames (USB Suspend)	4.9
		EDRX=20.48s, PTW=1.28s, DRX=1.28s (USB Disconnect)	4
		EDRX=20.48s, PTW=1.28s, DRX=1.28s (USB Suspend)	4.7
		EDRX=40.96s, PTW=1.28s, DRX=1.28s (USB Disconnect)	3.9
		EDRX=40.96s, PTW=1.28s, DRX=1.28s (USB Suspend)	4.7
		EDRX=81.92s, PTW=1.28s, DRX=1.28s (USB Disconnect)	3.9
		EDRX=81.92s, PTW=1.28s, DRX=1.28s (USB Suspend)	4.7
		EDRX=81.92s, PTW=2.56s, DRX=1.28s (USB Disconnect)	3.9
		EDRX=81.92s, PTW=2.56s, DRX=1.28s (USB Suspend)	4.7
I_{IDLE}	NR FDD	Paging cycle #64 frames (USB Disconnect)	13
		Paging cycle #64 frames (USB Connect)	21.5
		EDRX=81.92, PTW=2.56s, DRX=1.28s (USB Disconnect)	11.5
		EDRX=81.92, PTW=2.56s, DRX=1.28s (USB Connect)	21
	NR TDD	Paging cycle #64 frames (USB Disconnect)	13.5
		Paging cycle #64 frames (USB Connect)	22
		EDRX=81.92, PTW=2.56s, DRX=1.28s (USB Disconnect)	11.5
		EDRX=81.92, PTW=2.56s, DRX=1.28s (USB Connect)	21
	LTE FDD	Paging cycle #64 frames (USB Disconnect)	13
		Paging cycle #64 frames (USB Connect)	21.5
		EDRX=81.92, PTW=2.56s, DRX=1.28s (USB Disconnect)	12.5
		EDRX=81.92, PTW=2.56s, DRX=1.28s (USB Connect)	21
	LTE TDD	Paging cycle #64 frames (USB Disconnect)	13
		Paging cycle #64 frames (USB Connect)	21.5
		EDRX=81.92, PTW=2.56s, DRX=1.28s (USB Disconnect)	12.5
		EDRX=81.92, PTW=2.56s, DRX=1.28s (USB Connect)	21
I_{ACTIVE}	NR FDD	NR FDD Data transfer n1 @+23dBm	650
		NR FDD Data transfer n2 @+23dBm	650
		NR FDD Data transfer n3 @+23dBm	750
		NR FDD Data transfer n5 @+23dBm	650

		NR FDD Data transfer n7 @+23dBm	850
		NR FDD Data transfer n8 @+23dBm	600
		NR FDD Data transfer n12 @+23dBm	650
		NR FDD Data transfer n13 @+23dBm	650
		NR FDD Data transfer n14 @+23dBm	600
		NR FDD Data transfer n18 @+23dBm	700
		NR FDD Data transfer n20 @+23dBm	680
		NR FDD Data transfer n25 @+23dBm	670
		NR FDD Data transfer n26 @+23dBm	650
		NR FDD Data transfer n28 @+23dBm	650
		NR FDD Data transfer n30 @+23dBm	850
		NR FDD Data transfer n66 @+23dBm	700
		NR FDD Data transfer n70 @+23dBm	700
		NR FDD Data transfer n71 @+23dBm	650
	NR TDD	NR TDD Data transfer n38 @+23dBm	300
		NR TDD Data transfer n40 @+23dBm	300
		NR TDD Data transfer n41 @+23dBm	300
		NR TDD Data transfer n48 @+23dBm	300
		NR TDD Data transfer n77 @+23dBm	300
		NR TDD Data transfer n78 @+23dBm	300
		NR TDD Data transfer n79 @+23dBm	350
	LTE FDD	LTE FDD Data transfer Band 1 @+23dBm	690
		LTE FDD Data transfer Band 2 @+23dBm	680
		LTE FDD Data transfer Band 3 @+23dBm	760
		LTE FDD Data transfer Band 4 @+23dBm	680
		LTE FDD Data transfer Band 5 @+23dBm	700
		LTE FDD Data transfer Band 7 @+23dBm	850
		LTE FDD Data transfer Band 8 @+23dBm	650
		LTE FDD Data transfer Band 12 @+23dBm	680
		LTE FDD Data transfer Band 13 @+23dBm	700
		LTE FDD Data transfer Band 14 @+23dBm	600
		LTE FDD Data transfer Band 17 @+23dBm	680

		LTE FDD Data transfer Band 18 @+23dBm	650
		LTE FDD Data transfer Band 19 @+23dBm	630
		LTE FDD Data transfer Band 20 @+23dBm	680
		LTE FDD Data transfer Band 25 @+23dBm	750
		LTE FDD Data transfer Band 26 @+23dBm	680
		LTE FDD Data transfer Band 28 @+23dBm	650
		LTE FDD Data transfer Band 30 @+23dBm	790
		LTE FDD Data transfer Band 66 @+23dBm	700
		LTE FDD Data transfer Band 71 @+23dBm	650
	LTE TDD	LTE TDD Data transfer Band 34 @+23dBm	360
		LTE TDD Data transfer Band 38 @+26dBm	700
		LTE TDD Data transfer Band 39 @+23dBm	350
		LTE TDD Data transfer Band 40 @+26dBm	700
		LTE TDD Data transfer Band 41 @+26dBm	700
		LTE TDD Data transfer Band 42 @+26dBm	550
		LTE TDD Data transfer Band 43 @+26dBm	500
		LTE TDD Data transfer Band 48 @+23dBm	350

The above power consumption data is the average measured value, Due to different test condition and consistency, the data floating range is normal within 10%

6.3 Maximum Transmit Power

The maximum transmit power refers to the power at the antenna pin of the module at an ambient temperature of 25℃. You should fully consider the insertion loss on the RF path when designing, so as not to affect the TRP indicator due to excessive insertion loss. The following table describes the maximum transmit power of the FG132-M. 2 series module.

Table 20. Maximum transmit power

Mode	Band	TX power (dBm)	Comment
NR FDD	n1	23±2	10MHz Bandwidth, inner full
	n2	23±2	10MHz Bandwidth, inner full
	n3	23±2	10MHz Bandwidth, inner full

Mode	Band	TX power (dBm)	Comment
	n5	23±2	10MHz Bandwidth, inner full
	n7	23±2	10MHz Bandwidth, inner full
	n8	23±2	10MHz Bandwidth, inner full
	n12	23±2	10MHz Bandwidth, inner full
	n13	23±2	10MHz Bandwidth, inner full
	n14	23±2	10MHz Bandwidth, inner full
	n18	23±2	10MHz Bandwidth, inner full
	n20	23±2	10MHz Bandwidth, inner full
	n25	23±2	10MHz Bandwidth, inner full
	n26	23±2	10MHz Bandwidth, inner full
	n28	23±2	10MHz Bandwidth, inner full
	n30	23±2	10MHz Bandwidth, inner full
	n66	23±2	10MHz Bandwidth, inner full
	n70	23±2	10MHz Bandwidth, inner full
	n71	23±2	10MHz Bandwidth, inner full
NR TDD	n38	23±2	20MHz Bandwidth, inner full
	n40	23±2	20MHz Bandwidth, inner full
	n41	23±2	20MHz Bandwidth, inner full
	n48	23±2	20MHz Bandwidth, inner full
	n77	23±2	20MHz Bandwidth, inner full
	n78	23±2	20MHz Bandwidth, inner full
	n79	23±2	20MHz Bandwidth, inner full
LTE FDD	Band 1	23±2	10MHz Bandwidth, 1 RB
	Band 2	23±2	10MHz Bandwidth, 1 RB
	Band 3	23±2	10MHz Bandwidth, 1 RB
	Band 4	23±2	10MHz Bandwidth, 1 RB

Mode	Band	TX power (dBm)	Comment
	Band 5	23±2	10MHz Bandwidth, 1 RB
	Band 7	23±2	10MHz Bandwidth, 1 RB
	Band 8	23±2	10MHz Bandwidth, 1 RB
	Band 12	23±2	10MHz Bandwidth, 1 RB
	Band 13	23±2	10MHz Bandwidth, 1 RB
	Band 14	23±2	10MHz Bandwidth, 1 RB
	Band 17	23±2	10MHz Bandwidth, 1 RB
	Band 18	23±2	10MHz Bandwidth, 1 RB
	Band 19	23±2	10MHz Bandwidth, 1 RB
	Band 20	23±2	10MHz Bandwidth, 1 RB
	Band 25	23±2	10MHz Bandwidth, 1 RB
	Band 26	23±2	10MHz Bandwidth, 1 RB
	Band 28	23±2	10MHz Bandwidth, 1 RB
	Band 30	23±2	10MHz Bandwidth, 1 RB
	Band 66	23±2	10MHz Bandwidth, 1 RB
	Band 70	23±2	10MHz Bandwidth, 1 RB
	Band 71	23±2	10MHz Bandwidth, 1 RB
LTE TDD	Band 34	23±2	10MHz Bandwidth, 1 RB
	Band 38	26±2	10MHz Bandwidth, 1 RB
	Band 39	23±2	10MHz Bandwidth, 1 RB
	Band 40	26±2	10MHz Bandwidth, 1 RB
	Band 41	26±2	10MHz Bandwidth, 1 RB
	Band 42	26±2	10MHz Bandwidth, 1 RB
	Band 43	26±2	10MHz Bandwidth, 1 RB
	Band 48	23±2	10MHz Bandwidth, 1 RB

6.4 Receiving Sensitivity

The receiving sensitivity refers to the sensitivity at the antenna pin of the module at an ambient temperature of 25℃. You should fully consider the insertion loss on the RF path when designing, so as not to affect the TIS indicator due to excessive insertion loss.

Table 21. Dual-antenna receiving sensitivity (dBm)

Band	Sensitivity PRX	Sensitivity DRX	Sensitivity PRX+DRX	3GPP-Requirement
5G NR n1 (20M)	-95	-95.5	-98	-93.8
5G NR n2 (20M)	-95.5	-95.5	-98.5	-91.8
5G NR n3 (20M)	-95	-95.5	-98	-90.8
5G NR n5 (20M)	-96	-97	-99	-90.8
5G NR n7 (20M)	-94.5	-95.5	-98	-91.8
5G NR n8 (20M)	-95	-96	-99	-85.5
5G NR n12 (10M)	-98	-98	-101	-93.8
5G NR n13 (10M)	-98	-98	-101	-93.8
5G NR n14 (10M)	-98	-98	-101	-93.8
5G NR n18 (10M)	-98	-99	-102	/
5G NR n20 (20M)	-95	-96	-98.5	-89.8
5G NR n25 (20M)	-95.5	-95.5	-98.5	-90.3
5G NR n26 (20M)	-95	-96	-99	-87.6
5G NR n28 (20M)	-96.5	-96	-99.5	-90.8
5G NR n30 (10M)	-97.5	-97.5	-100	-95.8
5G NR n38 (20M)	-96	-95	-98	-93.8
5G NR n40 (20M)	-95	-95.5	-98	-93.8
5G NR n41 (20M)	-96	-95	-99	-91.8
5G NR n48 (20M)	-96	-96	-99.5	-92.8
5G NR n66 (20M)	-95	-95	-98.5	-93.3
5G NR n70 (15M)	-97	-96.5	-100	-95
5G NR n71 (20M)	-96	-95	-99	-86
5G NR n77 (20M)	-96	-96	-99	-92.3
5G NR n78 (20M)	-96	-94.5	-98.5	-92.8
5G NR n79 (20M)	-96	-95	-98.5	-92.8
LTE Band 1(10M)	-98	-98	-101	-96.3

Band	Sensitivity PRX	Sensitivity DRX	Sensitivity PRX+DRX	3GPP-Requirement
LTE Band 2(10M)	-98.5	-98.5	-101.5	-94.3
LTE Band 3(10M)	-98	-98	-101	-93.3
LTE Band 4(10M)	-98	-98	-101.5	-96.3
LTE Band 5(10M)	-98.5	-99.5	-102	-94.3
LTE Band 7(10M)	-97.5	-98	-100.5	-94.3
LTE Band 8(10M)	-98.5	-99	-102	-93.3
LTE Band 12(10M)	-98	-98	-101	-93.3
LTE Band 13(10M)	-98	-98	-101	-93.3
LTE Band 14(10M)	-98	-98	-101	-93.
LTE Band 17(10M)	-98	-98	-101.5	-93.3
LTE Band 18(10M)	-98.5	-99	-102	-96.3
LTE Band 19(10M)	-98.5	-99	-102	-96.3
LTE Band 20(10M)	-98.5	-99	-102	-93.3
LTE Band 25(10M)	-98.5	-98	-101.5	-92.8
LTE Band 26(10M)	-98.5	-99	-102	-93.8
LTE Band 28(10M)	-99	-99	-102	-94.8
LTE Band 30(10M)	-97.5	-97	-100.5	-95.3
LTE Band 34(10M)	-98	-98	-100.5	-96.3
LTE Band 38(10M)	-98.5	-97	-100.5	-96.3
LTE Band 39(10M)	-98	-98.5	-101	-96.3
LTE Band 40(10M)	-97	-97.5	-100	-96.3
LTE Band 41(10M)	-98.5	-97.5	-100.5	-94.3
LTE Band 42(10M)	-99	-98	-101.5	-95
LTE Band 43(10M)	-99	-98	-101.5	-95
LTE Band 48(10M)	-99	-98	-101.5	-95
LTE Band 66(10M)	-98	-98	-101	-95.8
LTE Band 71(10M)	-99.5	-98	-101.5	-93.5

6.5 GNSS

The module supports multiple positioning systems including GPS/Beidou/GLONASS/Galileo/QZSS. The module is embedded with LNA, which can effectively improve the sensitivity of GNSS. Test conditions: Power supply voltage 3.8V, ambient temperature 25°C.

Table 22. GNSS performance

Parameter	Description (instrument test)	Typical Result	Unit
Sensitivity	Acquisition	-146	dBm
	Tracking	-157	dBm
C/N	-130dBm	38.5	dB-Hz
TTFF	Cold Start @all sky	26.67	s
	A-GPS @all sky	9.49	s
	Warm Start @all sky	21.12	S
	Hot Start @all sky	1	S
Static accuracy	CEP-50 @all sky	1.81	m

Table 23. GNSS band

Mode	Band	Unit
GPS/QZSS	L1: 1575.42	MHz
	L5: 1176.45	MHz
GLONASS	L1: 1602	MHz
Beidou	B1I: 1561.098	MHz
	B1C: 1575.42	MHz
	B2A: 1176.45	MHz
Galileo	E1: 1575.42±2.046	MHz
	E5a: 1176.45±10.23	MHz

6.6 Electrostatic Protection

The FG132-M.2 module is a precise electronic product. If ESD protection measures are not taken, a permanent damage may be caused to the module. ESD protection measures should be taken in various links such as R&D debugging, production and assembly, and testing. Therefore, in addition to ESD protection on the package, customers should refer to the recommended design circuits of each interface as much as possible. The following figure shows the ESD protection levels at an ambient temperature of 25℃ and a humidity of 45%.

Table 24. ESD protection levels

Location	Air Discharge	Contact Discharge
GND	±15 kV	±8 kV
Antenna interface	- -	±8 kV
Other interfaces	±1 kV	±0.5 kV

- The data is tested based on Fibocom development board.
- The ESD performance is strongly related to PCB design. Pay special attention to the protection of control signals.
- When designing the whole machine, the GND of the module and the main GND of the large board should maintain sufficient connectivity to ensure that the ESD is discharged through the shortest path.

6.7 Reliability Test

Fibocom reliability test is carried out at the industrial level. The following table describes the test results of each project.

Table 25. Reliability test results

Test Item	Test Condition
High temperature aging	85°C, 168H/504H/1008H
High temperature and humidity	85°C , 85%RH, 168H/504H/1008H
Corner test	High and low temperature, high and low humidity, high and low voltage, six groups of combinations, and each combination runs for 24 hours
Temperature shock	90/-45°C, 200C
Random vibration	Frequency range: 200Hz to 2000Hz, PSD=0.04 g2/Hz, one hour for X/Y/Z axis
Monomer drop	1m, 6 sides and 2 wheels
Mechanical collision	Peak acceleration: 180m/s2 Pulse duration: 6ms Number of collisions: 1000
Low temperature boot	-40°C, 30 minutes off/5 minutes idle, 3 days
Condensation test	3 days (3 cycles): • First and second cycles with cold cycle • Third cycle without cold cycle
Temperature cycle	85°C/-40°C; 10°C/min; 10min; 240 cycles
Sinusoidal vibration	Amplitude: 3.0G peak to peak Frequency: 5Hz to 500Hz Sweep frequency: 0.5 Octave/min, linear Each axis: 2H
Salt spray	Neutral salt spray, 48H

6.8 Thermal Design

The MiniPCIe structure of the FG132 is connected to the motherboard by inserting a MiniPCIe connector, and the tail is fixed to the motherboard with screws. Its PCB size is small, the heat dissipation capacity is poor, it is recommended to use the motherboard PCB or radiator to dissipate heat to the outside world, there are two main ways of heat dissipation: bottom PCB heat dissipation and top shield heat dissipation.

(1) Bottom PCB heat dissipation: according to the size of the selected MiniPCIe connector, calculate the gap between the MiniPCIe baseplate and the motherboard, and select the appropriate thickness of the thermal gasket (thermal gasket recommended 20% compression rate). For example, if the connector is Molex MiniPCI Express connector, the model is: 67910-0002, the gap between the MiniPCIe baseplate and the mainboard is 1.6mm. You are advised to select a thermal pad with a thickness of 2mm. The MiniPCIe baseplate, thermal pad, and mainboard must be in close contact with each other. At the same time, the projection position of the main board increases the cooling surface (exposed copper); Add the hole, the hole is plated with copper; Increase the copper thickness ratio in the thickness direction; Heat dissipation measures such as the contact between the mainboard and the shell.

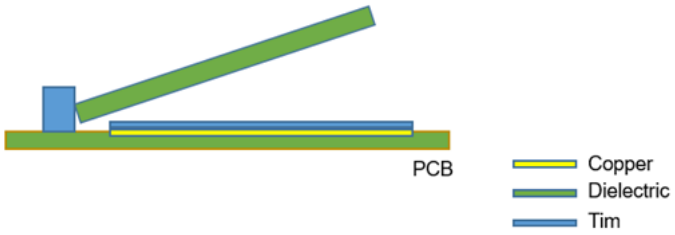


Figure 14. Heat dissipation between MiniPCIe and motherboard PCB

(2) Top shielding cover heat dissipation: the outer surface of the top shielding cover of the module is affixed with thermal shims, and the heat sink is installed above the thermal shims. The heat sink, thermal shims and module shielding cover are required to be in close contact with each other. The thermal shims are recommended to have a compression rate of 20%. If the shell has no ergonomic requirements, the module shield can also be used to contact the shell, which is conducive to rapid heat dissipation, and the contact part of the shell is filled with thermal adhesive or thermal gasket.

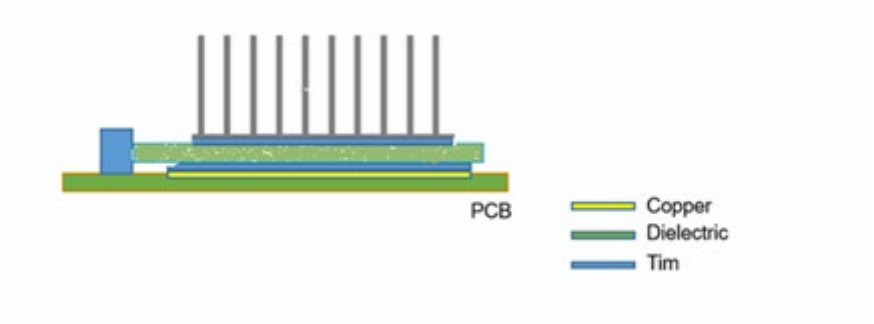


Figure 15. Heat dissipation of module shield

Material selection suggestions refer to the following table:

Table 26. Selection of cooling materials

Material Type	Selection Suggestion
Radiator material	ADC12, AL6061, AL6063, AL5051, AL7075 aluminum alloy, aluminum alloy surface is oxidized or painted, the size and shape can be customized according to the customer's application scenario
Thermal gasket	The thermal conductivity is recommended at 4W/(m·K) and above, and the three-way thermal gel is recommended, the model is SY-TP652-3
coupler	Mini PCI Express connector from Molex, model number: 67910-0002

7 Structure Specifications

7.1 Product Appearance

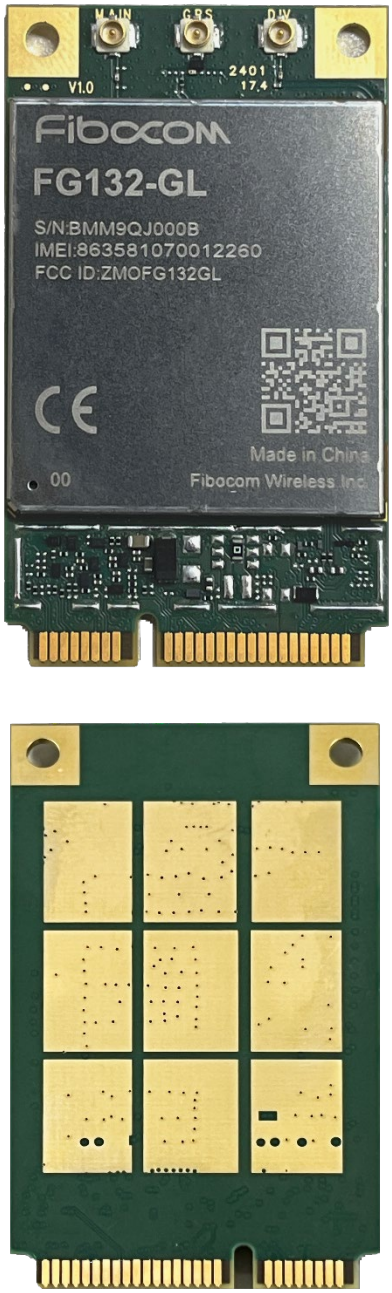


Figure 16. Product appearance

The figures are for reference only. Please refer to the actual product for details

7.2 Structure Dimensions

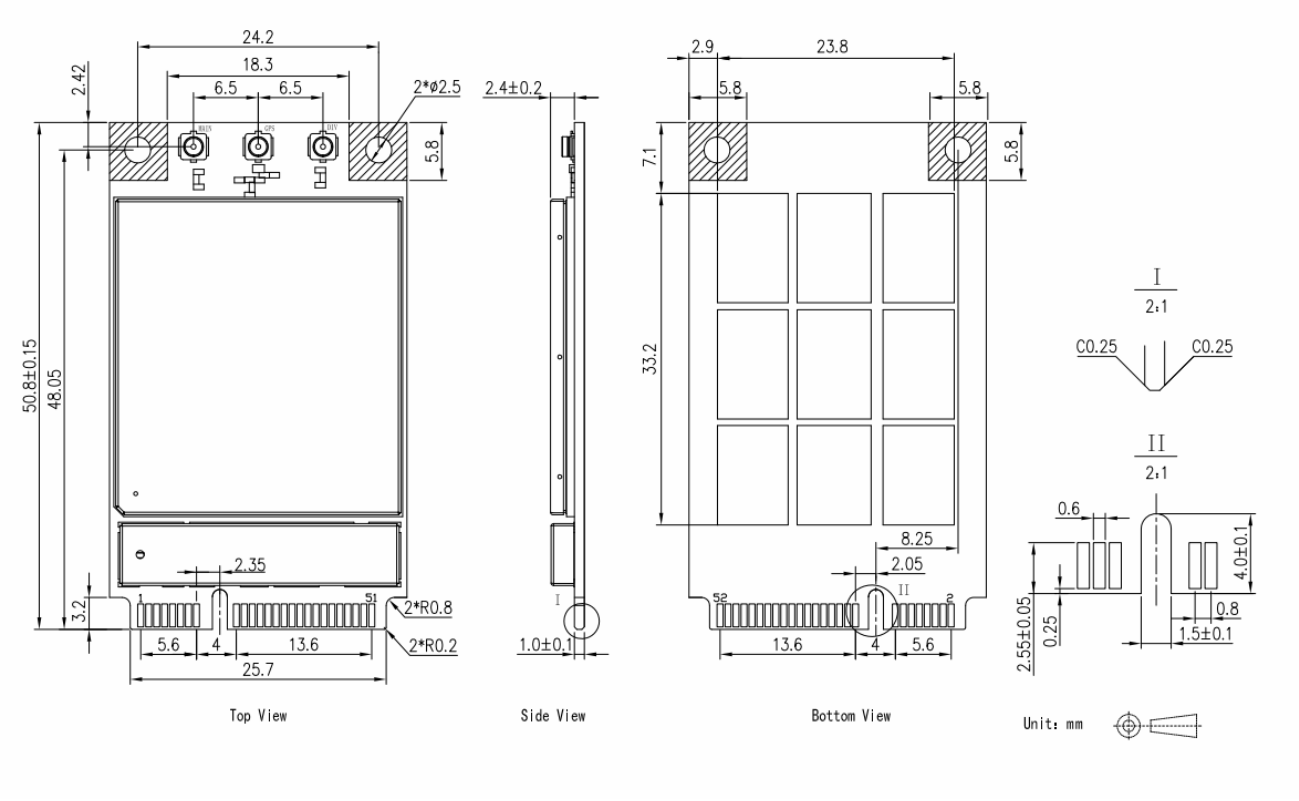


Figure 17. Structure dimensions (unit: mm)

7.3 MiniPCIe Connector

Connectors that meet PCI Express Mini Card standards can be used with this module. Molex 67910-0002 connectors are recommended, as shown in the following figure:

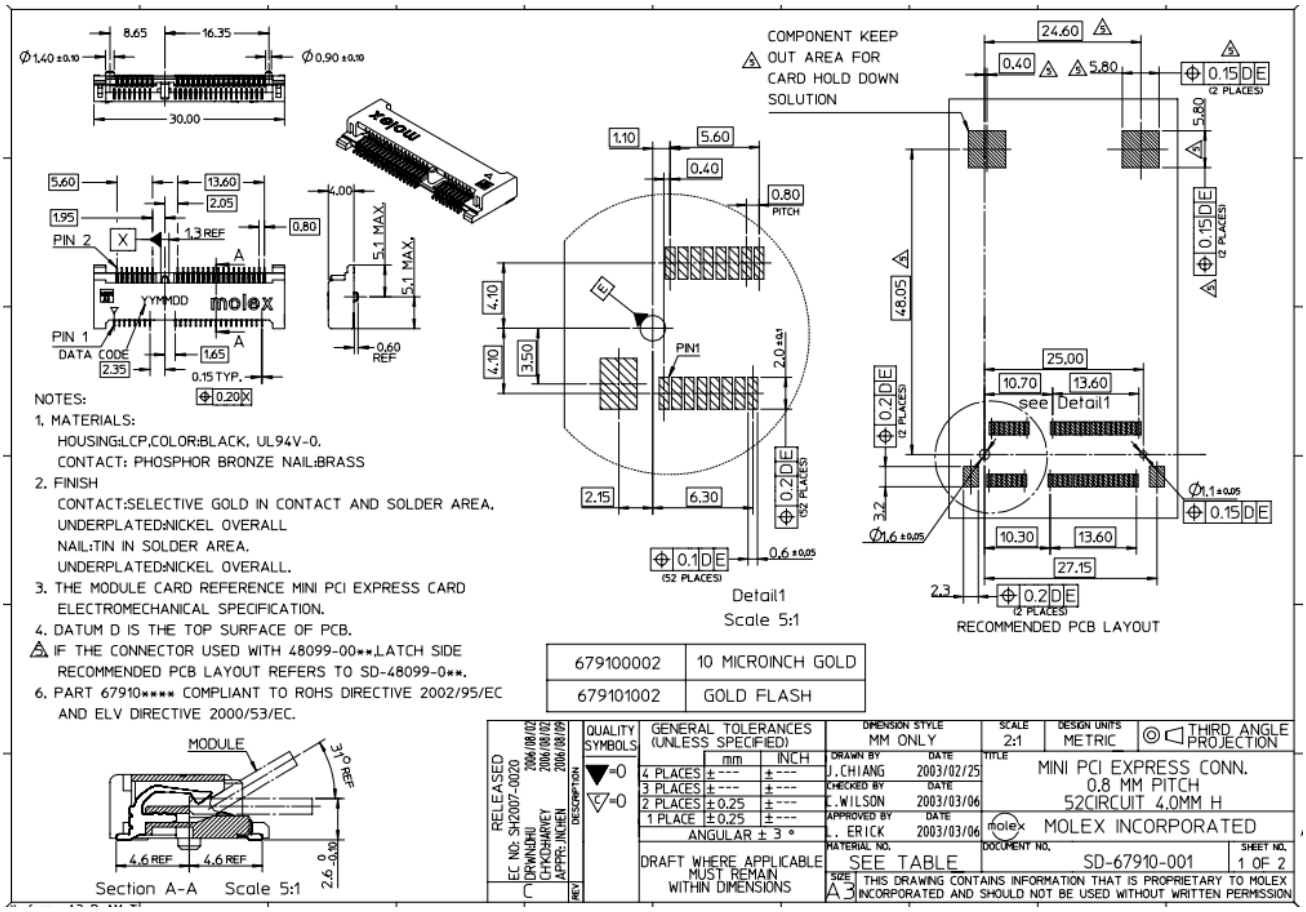


Figure 18. MiniPCIe connector dimensions

8 Storage and Packaging

8.1 Storage Conditions

Modules are shipped in vacuum sealed bags. The module has a humidity sensitivity level of 3 (MSL 3) and is stored in accordance with the following conditions:

- Storage conditions (recommended) : Temperature 23°C ± 5°C, relative humidity RH 35%~70%;
- Storage period (sealed vacuum packaging): Under recommended storage conditions, the storage period is 12 months.

8.2 Packaging Specifications

The module is packed in pallet-sealed packaging, with 20pcs in each disc and 6 discs in each box (the top layer is an empty tray), a total of 100pcs, and 6 boxes in each box. Combined with the outer packaging mode of the hard cartoon box, the storage, transportation and use of the module play a maximum protective role.

Pallet size: 315 mm x 170 mm x 6.5 mm, the specific size is shown below:

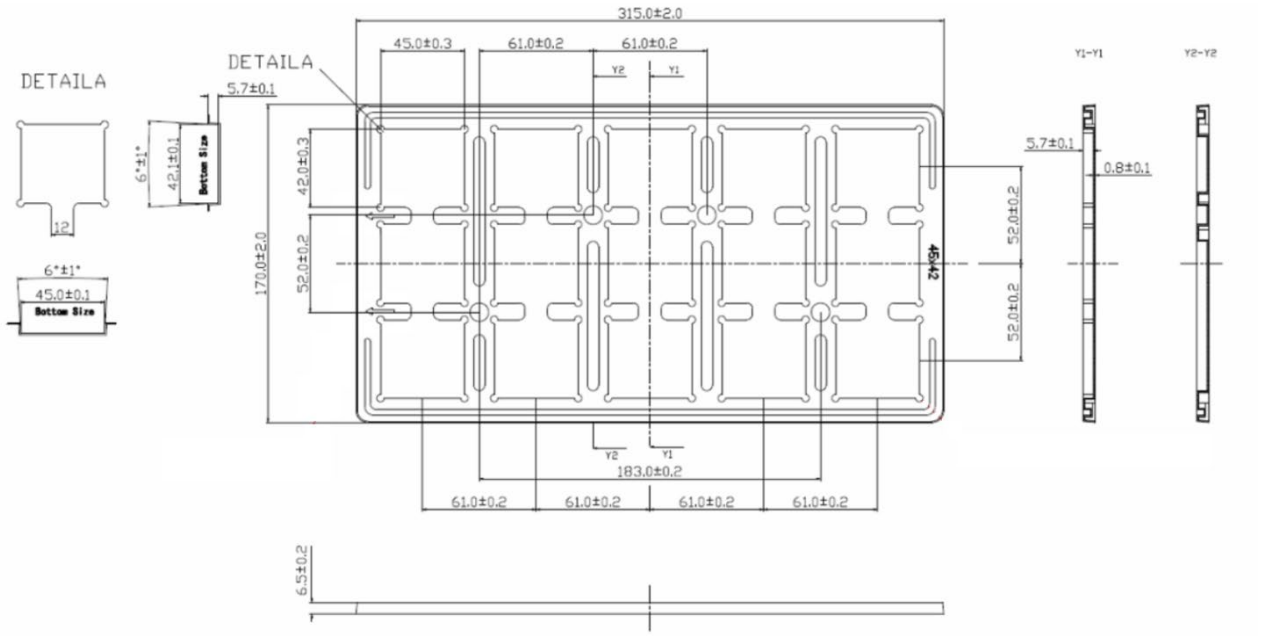


Figure 19. Tray dimensions (unit: mm)

Appendix A References

Fibocom provides the following related documents for your reference. If you have other requirements, please call Fibocom FAE.

Category	Document Name
Software	Fibocom_FG132_AT Commands User Manual
Development suite	Fibocom_EVK-GT8230-NL_User Guide_V1.0.5
Other	Fibocom_General Thermal Design Guide for modules

Appendix B Acronyms and Abbreviations

Acronym and Abbreviation	Description
bps	Bits Per Second
CA	Carrier Aggregation
CAT	Category
CPE	Customer Premise Equipment
DRX	Discontinuous Reception
DL	Downlink
DLCA	Downlink Carrier Aggregation
ECC	Envelope Correlation Coefficient
EN-DC	E-UTRA New Radio-Dual Connectivity
FDD	Frequency Division Duplexing
HB	High Band
HSDPA	High Speed Down Link Packet Access
GNSS	Global Navigation Satellite System
GPS	Global Positioning System
Imax	Maximum Load Current
LB	Low Band
LED	Light Emitting Diode
LSB	Least Significant Bit
LTE	Long Term Evolution
MB	Middle Band
ME	Mobile Equipment
MIMO	multiple-input and multiple-output
MS	Mobile Station
MT	Mobile Terminated
NR	New Radio
NSA	Non-Standalone
PA	Power Amplifier
PCB	Printed Circuit Board
PDU	Protocol Data Unit

Acronym and Abbreviation	Description
PSK	Phase Shift Keying
QAM	Quadrature Amplitude Modulation
QPSK	Quadrature Phase Shift Keying
QZSS	Quasi-Zenith Satellite System
RF	Radio Frequency
RHCP	Right Hand Circularly Polarized
RMS	Root Mean Square
RTC	Real Time Clock
Rx	Receive
SA	Standalone
SCell	Secondary Cell for CA
SMS	Short Message Service
TE	Terminal Equipment
TX	Transmitting
TT	Test Tolerance
TDD	Time Division Duplexing
UART	Universal Asynchronous Receiver & Transmitter
UL	Uplink
UMTS	Universal Mobile Telecommunications System
URC	Unsolicited Result Code
USIM	(Universal) Subscriber Identity Module
VSWR	Voltage Standing Wave Ratio